IN THE SPECIFICATION

Please replace the paragraph beginning at page 4, line 1, with the following amended paragraph:

The present invention in the illustrative embodiment provides an efficient and flexible scheduler architecture capable of supporting multiple scheduling algorithms. The architecture is particularly advantageous in the network processor context in that it provides sufficient flexibility to allow the implementation of new algorithms as they are defined without requiring redesign of the hardware or other elements of the network processor. A single network processor design can thus be used in a wide variety of processing applications. In the illustrative embodiment, this may be accomplished utilizing a combination of a work-conserving bandwidth sharing mechanism and a non-work-conserving explicit rate establishment mechanism.

Please replace the paragraph beginning at page 10, line 21, with the following amended paragraph:

The dynamic calendar table 312 in the illustrative embodiment comprises a calendar table that is configured such that each of the plurality of queues [[to]] can be dynamically assigned a transmission rate. Initially, prior to the scheduling of any queue, the calendar table is empty. The scheduler 300 maintains a pointer, denoted CurrentPointer, that is incremented with every pulse of a scheduling clock or other time base of the scheduler. The calendar table includes a plurality of slots, with each slot capable of storing the identifier of one of the queues.

Please replace the paragraph of the abstract beginning at page 20, line 2, with the following amended paragraph:

A processor includes a scheduler operative to schedule data blocks for transmission from a plurality of queues or other transmission elements, utilizing at least a first table and a second table. The first table may comprise at least first and second first-in first-out (FIFO) lists of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with a first scheduling algorithm, such as a weighted fair queuing scheduling algorithm. The scheduler maintains a first table pointer identifying at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table. The second table includes a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with a second scheduling algorithm, such as a constant bit rate or variable bit rate scheduling algorithm. ~~Association of a given one of the transmission elements with a particular one of the second table entries establishes a scheduling rate for that transmission element. The scheduler maintains a second table pointer identifying a current one of the second table entries that is eligible for transmission.~~